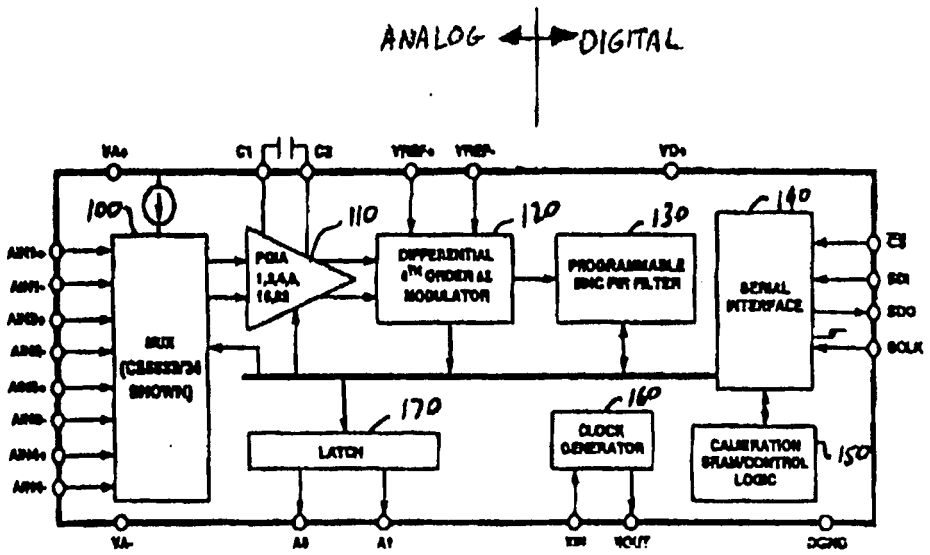
ANALOG
DIGITAL
VA+
C1
C2
VREF+
VREF-
VD+
100
110
120
130
140
150
160
170
PGIA
DIFFERENTIAL
PROGRAMMABLE
SERIAL
INTERFACE
MUX
LATCH
CLOCK
GENERATOR
CS
SDI
SDO
SCLK
VA-
AGND
VOUT
DGND

FIGURE 1.1

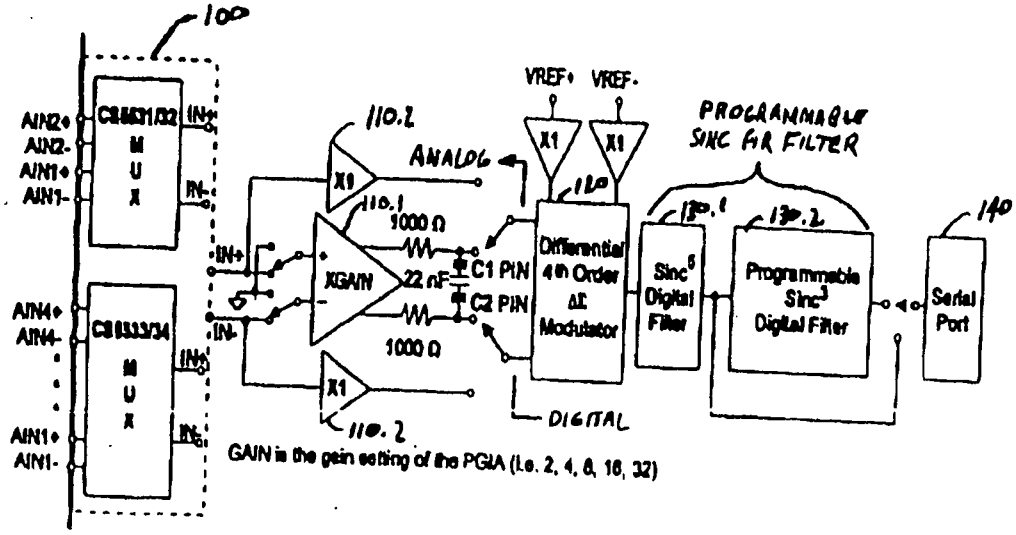
100
AIN2+
AIN2-
AIN1+
AIN1-
MUX
AIN4+
AIN4-
AIN1+
AIN1-
MUX
IN+
IN-
110.2
X1
ANALOG
110.1
1000 Ω
XGAIN
22 nF
C1 PIN
C2 PIN
1000 Ω
X1
110.2
VREF+
VREF-
X1
X1
110
PROGRAMMABLE SINC FIR FILTER
130.1
130.2
Differential 4th Order ΔΣ Modulator
Sinc5 Digital Filter
Programmable Sinc3 Digital Filter
140
Serial Port
DIGITAL
GAIN is the gain setting of the PGIA (i.e. 2, 4, 8, 16, 32)

FIGURE 1.2

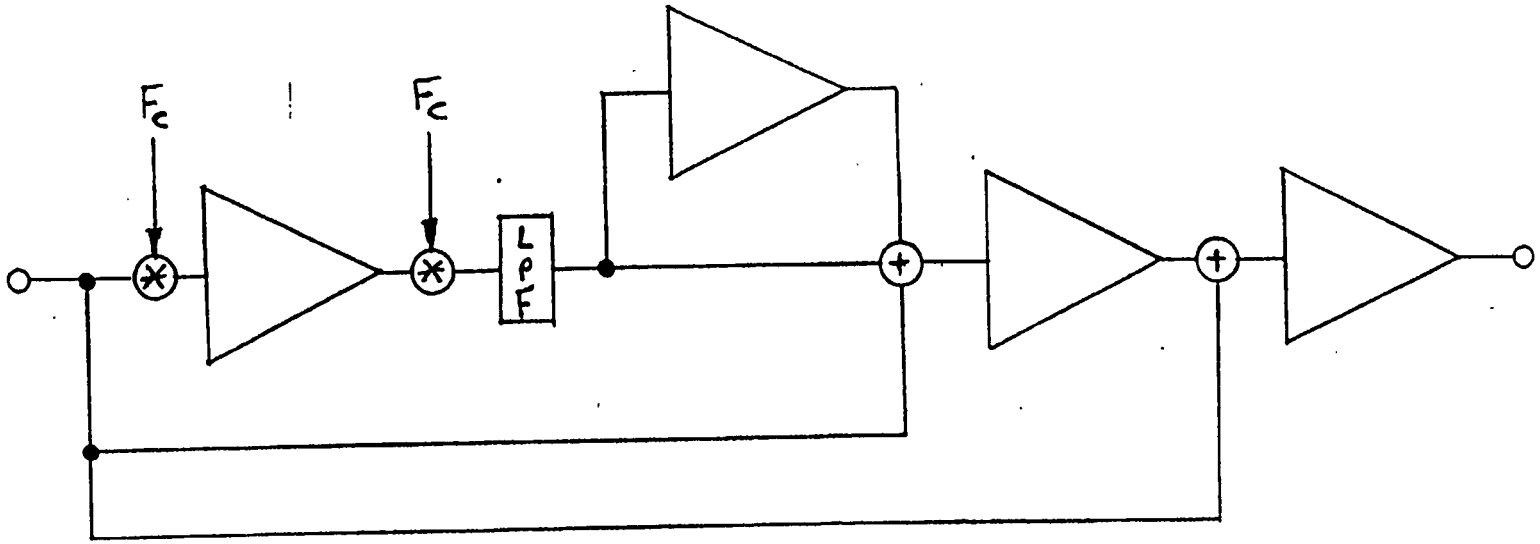

FIGURE 1.3

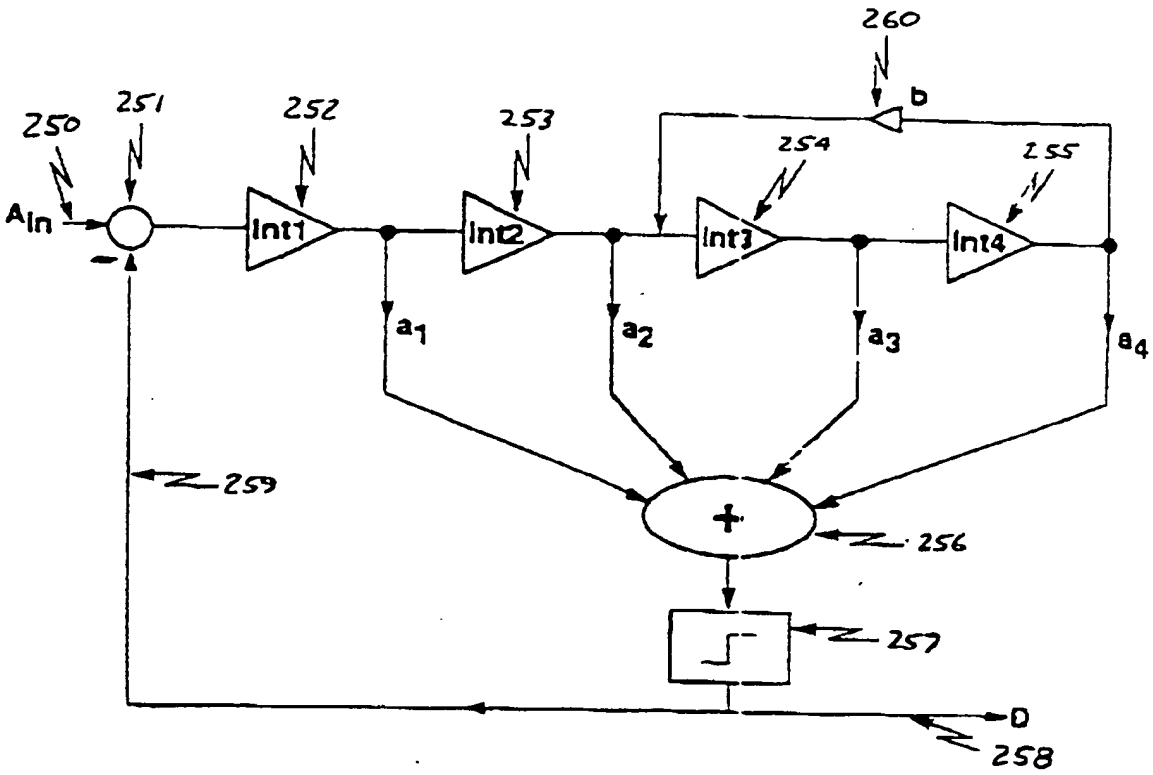

Figure 1.4

0055205 "09/55/60

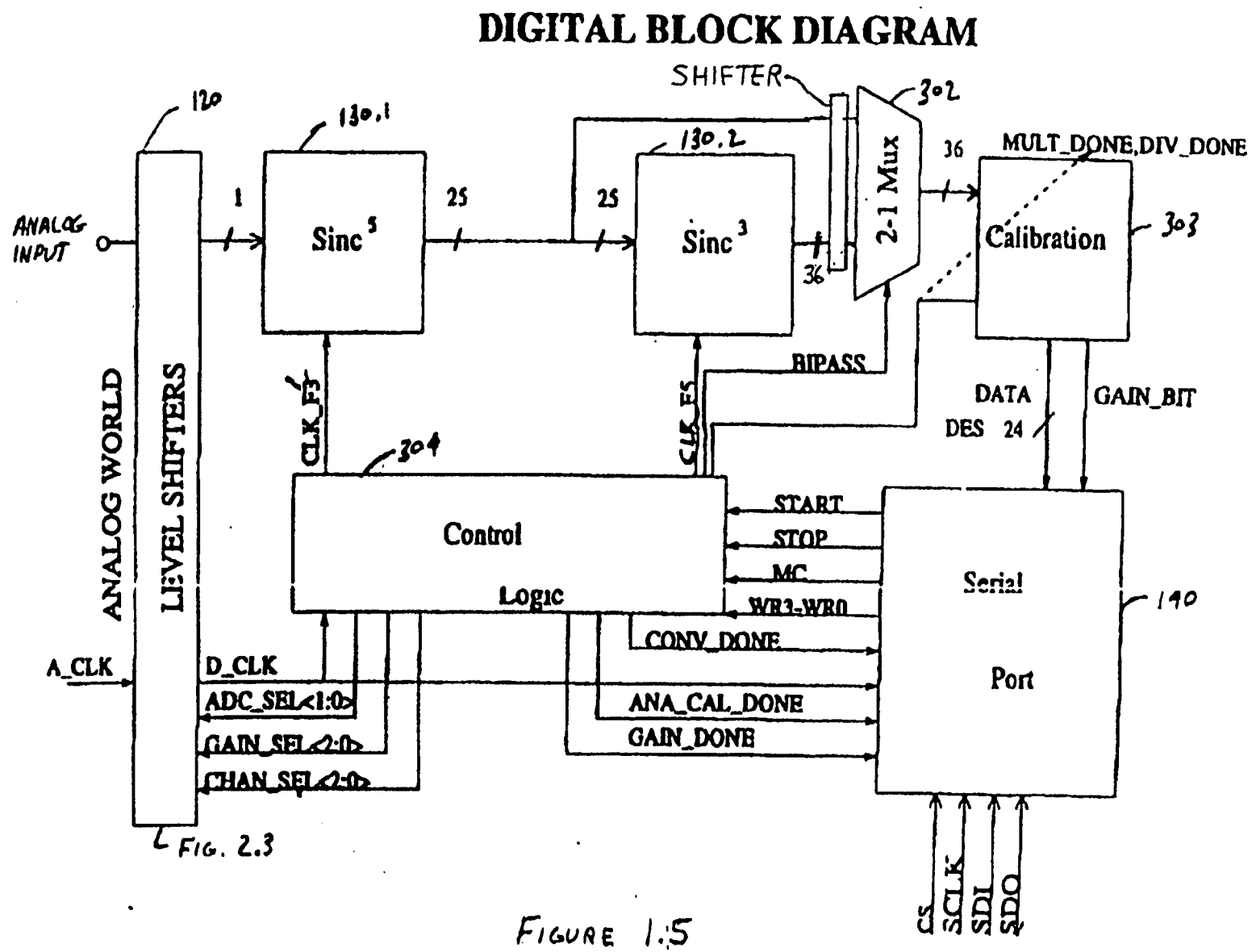

FIG. 2.3

FIGURE 1.5

005207 "90256960

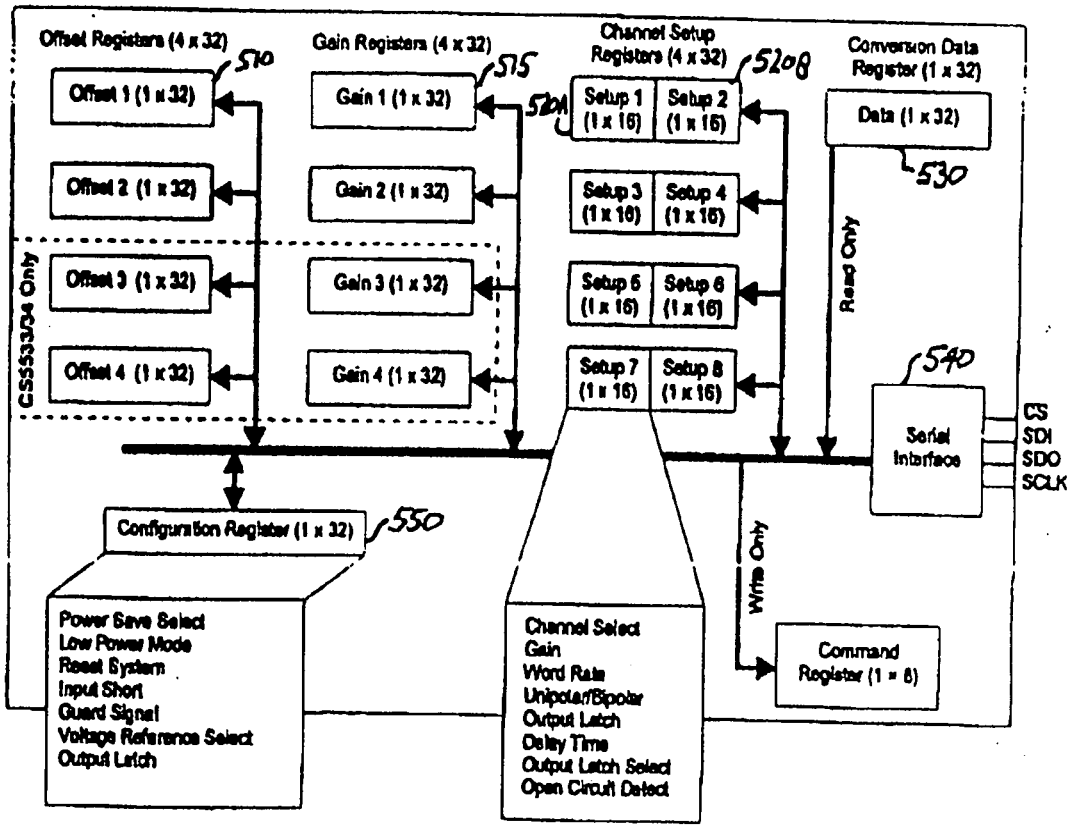

FIGURE 1.6

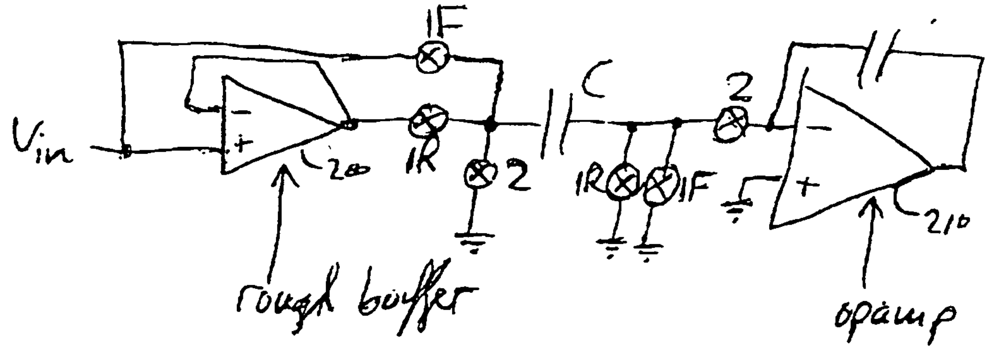

FIGURE 2.0

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DO NOT COPY

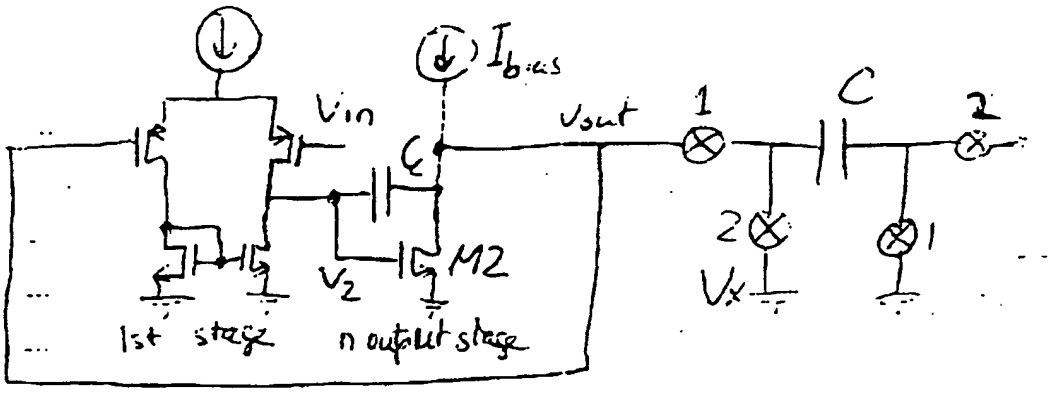


FIGURE 2.1

V_{IN} = CONSTANT

$V_{OUT} > V_X$

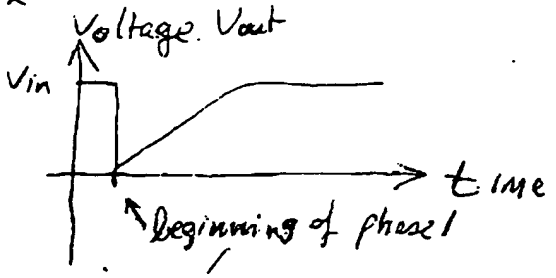


FIGURE 2.2

SCANNED, # 14

V_{IN} = CONSTANT

$V_{OUT} < V_X$

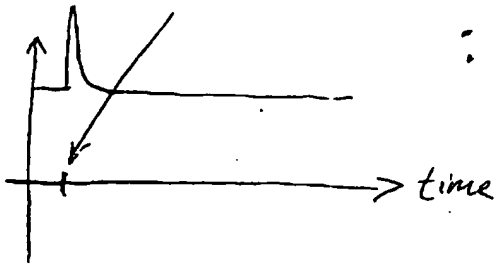


FIGURE 2.3

0052207-900526960

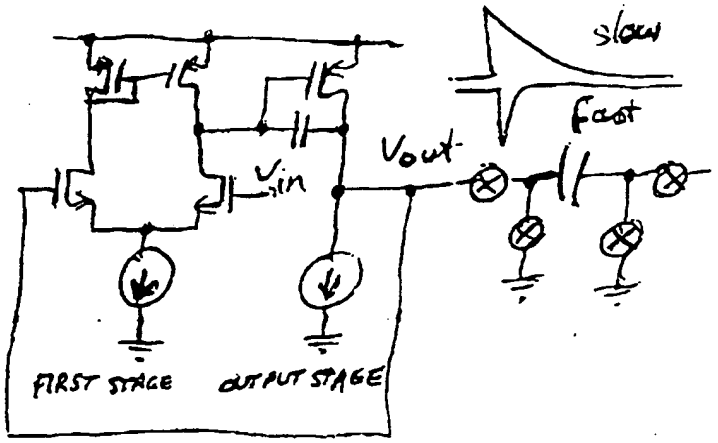


FIGURE 2.4

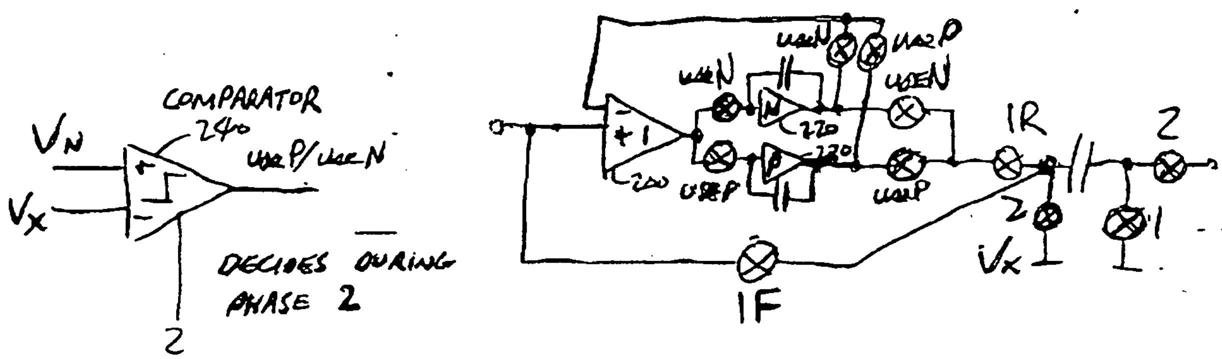


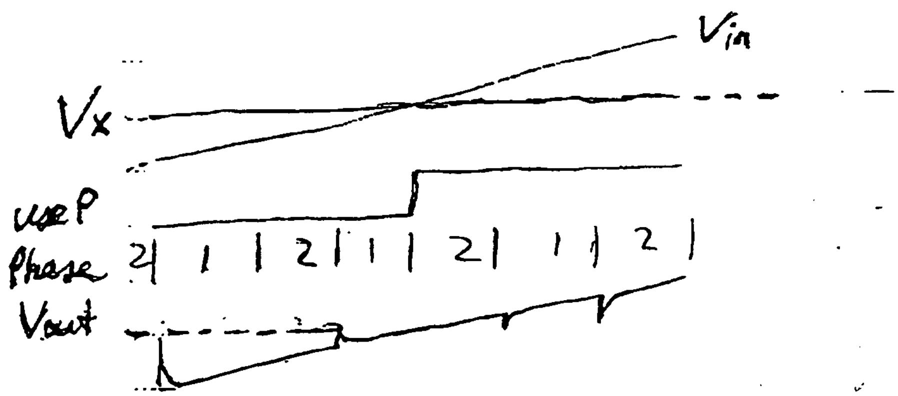
FIGURE 2.5

09625706 . 102500

FIGURE 2.6

FIGURE 2.7

FIGURE 2.8



MULTIPLIER ARCHITECTURE

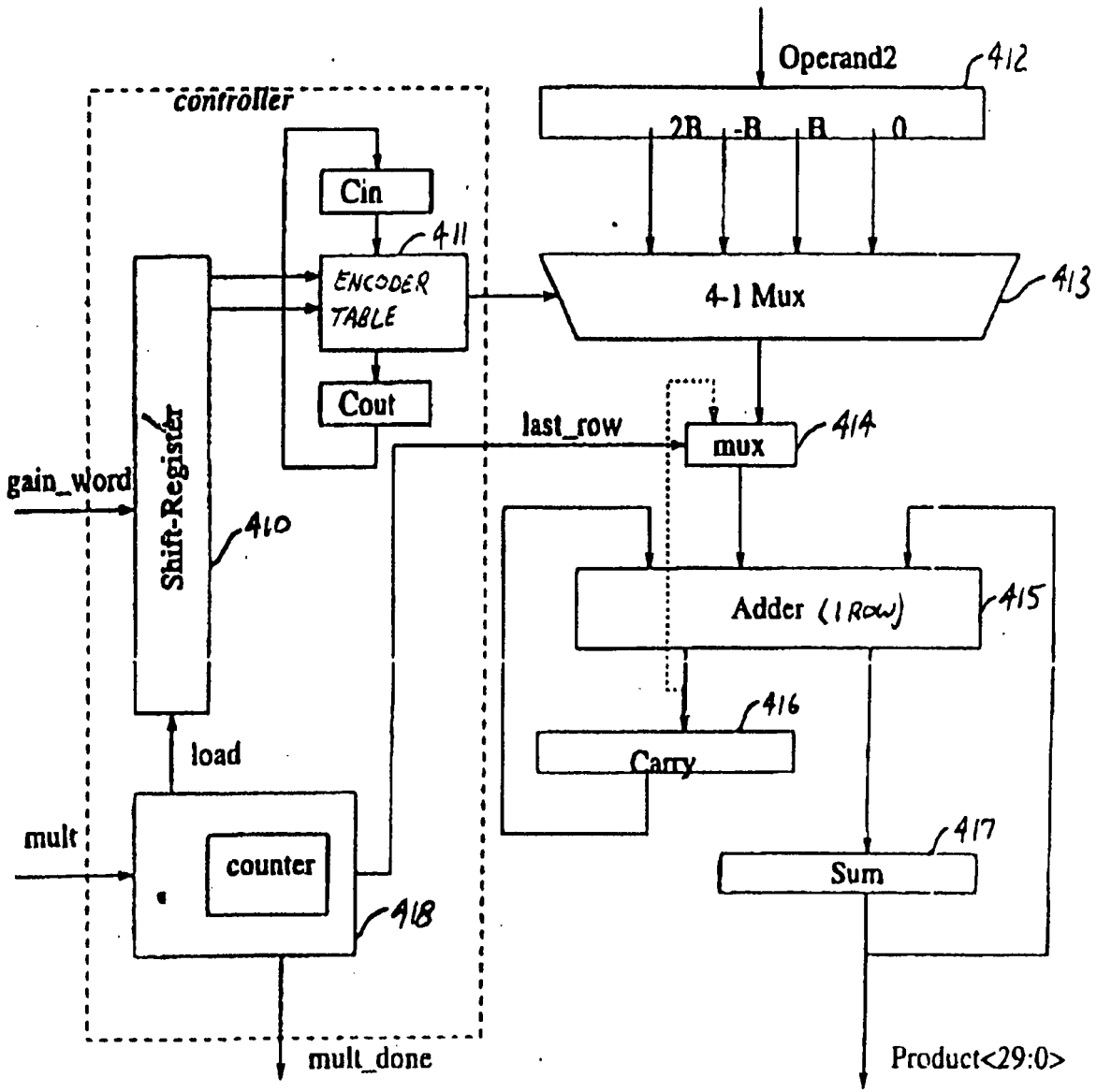


FIGURE 3.1

Multiplication

FIGURE 3.2
(PRIOR ART)

Table 2: Encoding Scheme Proposed

A_{i+1}	A_i	Operation
0	0	$R_i = R_{i-1}/4$
0	1	$R_i = (R_{i-1} + B)/4$
1	0	$R_i = (R_{i-1} + 2B)/4$
1	1	$R_i = (R_{i-1} + 3B)/4$

FIGURE 3.3
(PRIOR ART)

Table 3: Carry Propagate Encoding Scheme

C_{in}	A_{i+1}	A_i	Operation	C_{out}
0	0	0	$R_i = R_{i-1}/4$	0
0	0	1	$R_i = (R_{i-1} + B)/4$	0
0	1	0	$R_i = (R_{i-1} + 2B)/4$	0
0	1	1	$R_i = (R_{i-1} - B)/4$	1
1	0	0	$R_i = (R_{i-1} + B)/4$	0
1	0	1	$R_i = (R_{i-1} + 2B)/4$	0
1	1	0	$R_i = (R_{i-1} - B)/4$	0
1	1	1	$R_i = (R_{i-1})/4$	1

Multiplication

FIGURE 3.4

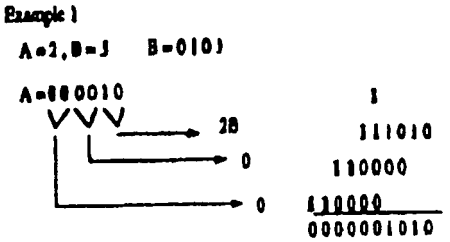
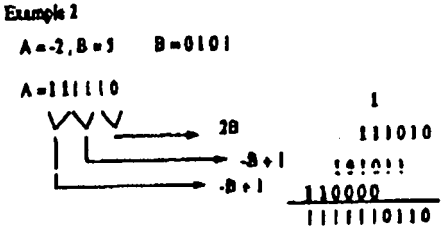


FIGURE 3.5



DOCKET 90/456,960

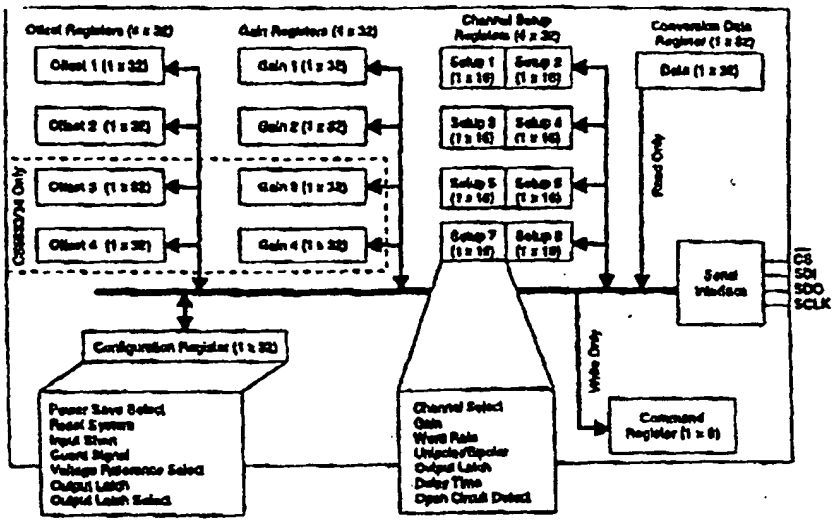


FIGURE 4.1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/$\overline{W}$	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	Must be logic 0 for these commands.
		1	These commands are invalid if this bit is logic 1.
D6	Access Registers as Arrays, ARA	0	Ignore this function.
		1	Access the respective registers, offset, gain, or channel-setup, as an array of registers. The particular registers accessed are determined by the RS bits. The registers are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0	00	CS1-CS0 provide the address of one of the two (four for CS5533/34) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.
		01	
		10	
		11	
D3	Read/$\overline{\text{Write}}$, R/$\overline{W}$	0	Write to selected register.
		1	Read from selected register.
D2-D0	Register Select Bit, RSB3-RSB0	000	Reserved
		001	Offset Register
		010	Gain Register
		011	Configuration Register
		100	Conversion Data Register (Read Only)
		101	Channel-Setup Registers
		110	Reserved
		111	Reserved

FIGURE 4.2

CS5532-AS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	These commands are invalid if this bit is logic 0.
		1	Must be logic 1 for these commands.
D6	Multiple Conversions, MC	0	Perform fully settled single conversions.
		1	Perform conversions continuously.
D5-D3	Channel-Setup Register Pointer Bits, CSRP	000 ... 111	These bits are used as pointers to the Channel-Setup registers. Either a single conversion or continuous conversions are performed on the channel setup register pointed to by these bits.
D2-D0	Conversion/Calibration Bits, CC2-CC0	000	Normal Conversion
		001	Self-Offset Calibration
		010	Self-Gain Calibration
		011	Reserved
		100	Reserved
		101	System-Offset Calibration
		110	System-Gain Calibration
		111	Reserved

FIGURE 4.3

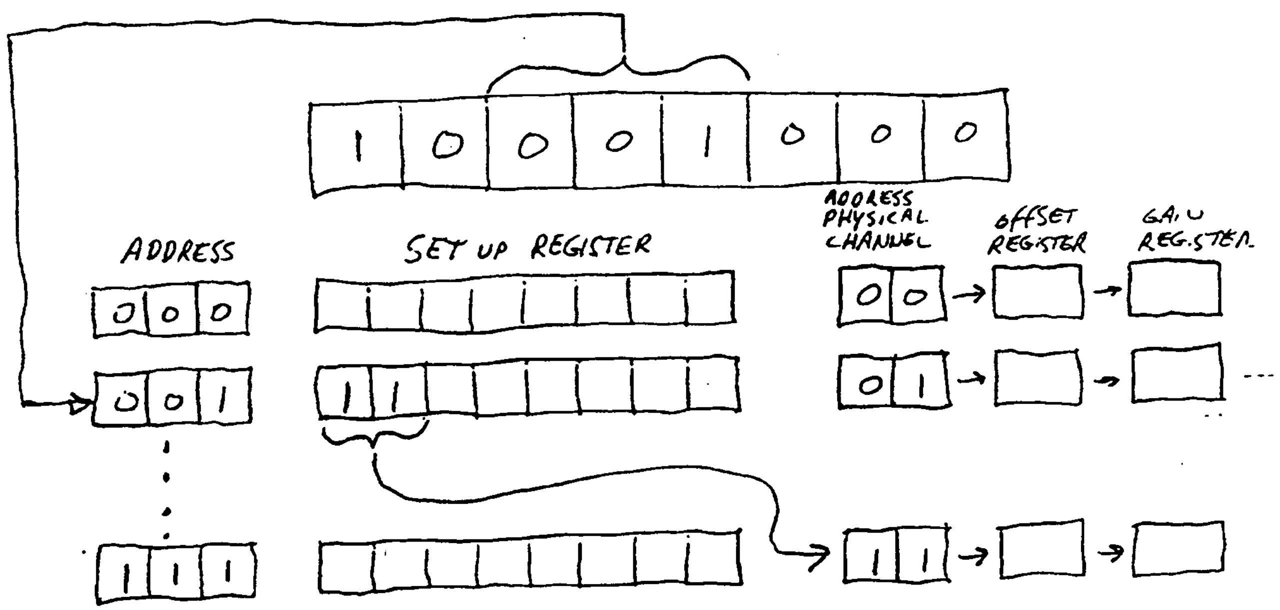


FIGURE 4.4

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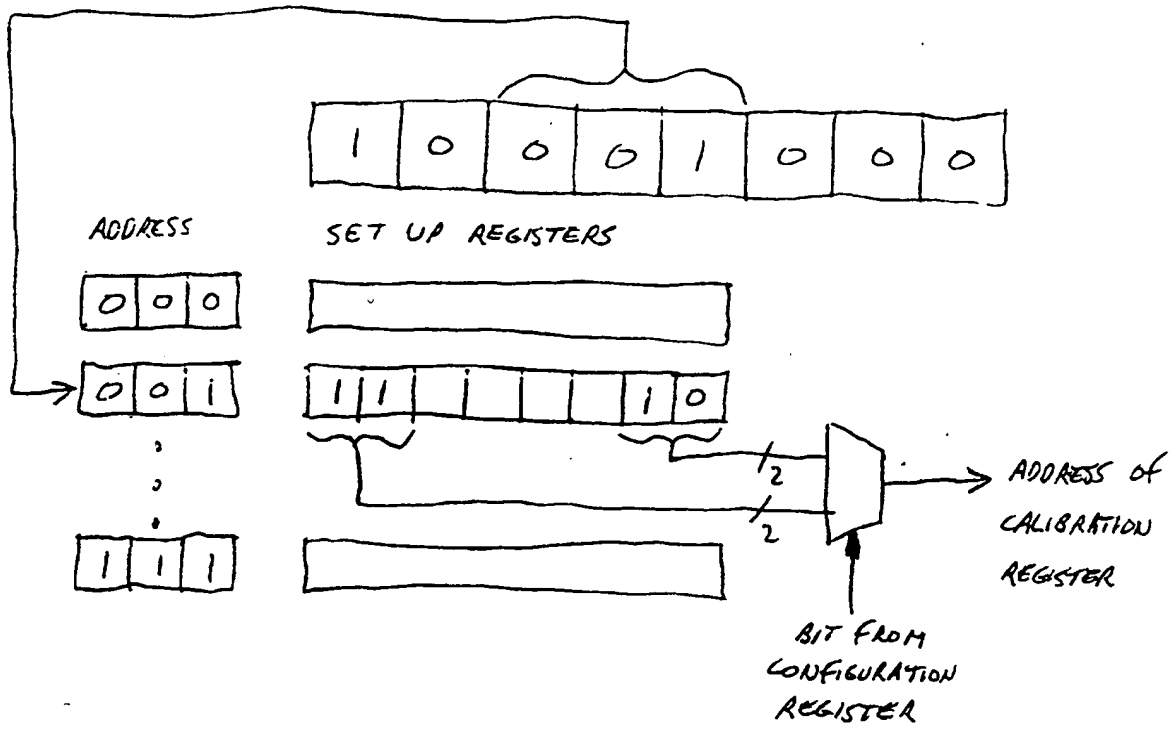

FIGURE 4.5

DO NOT SCALE DRAWING

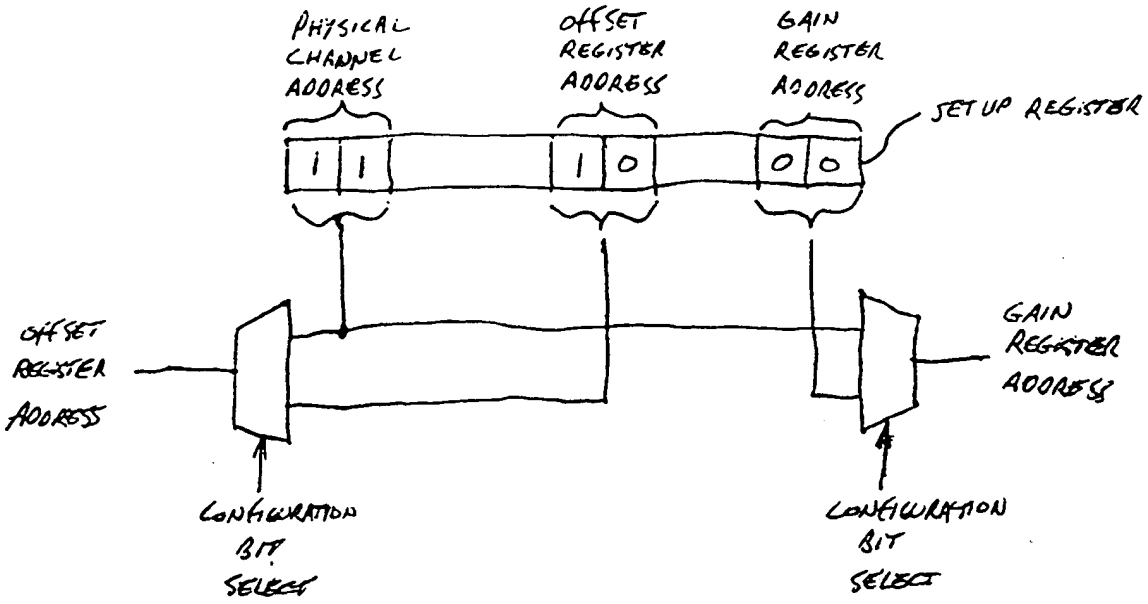
PHYSICAL CHANNEL ADDRESS
OFFSET REGISTER ADDRESS
GAIN REGISTER ADDRESS
SET UP REGISTER
1 1
1 0
0 0
OFFSET REGISTER ADDRESS
GAIN REGISTER ADDRESS
CONFIGURATION BIT SELECT
CONFIGURATION BIT SELECT

FIGURE 4.6

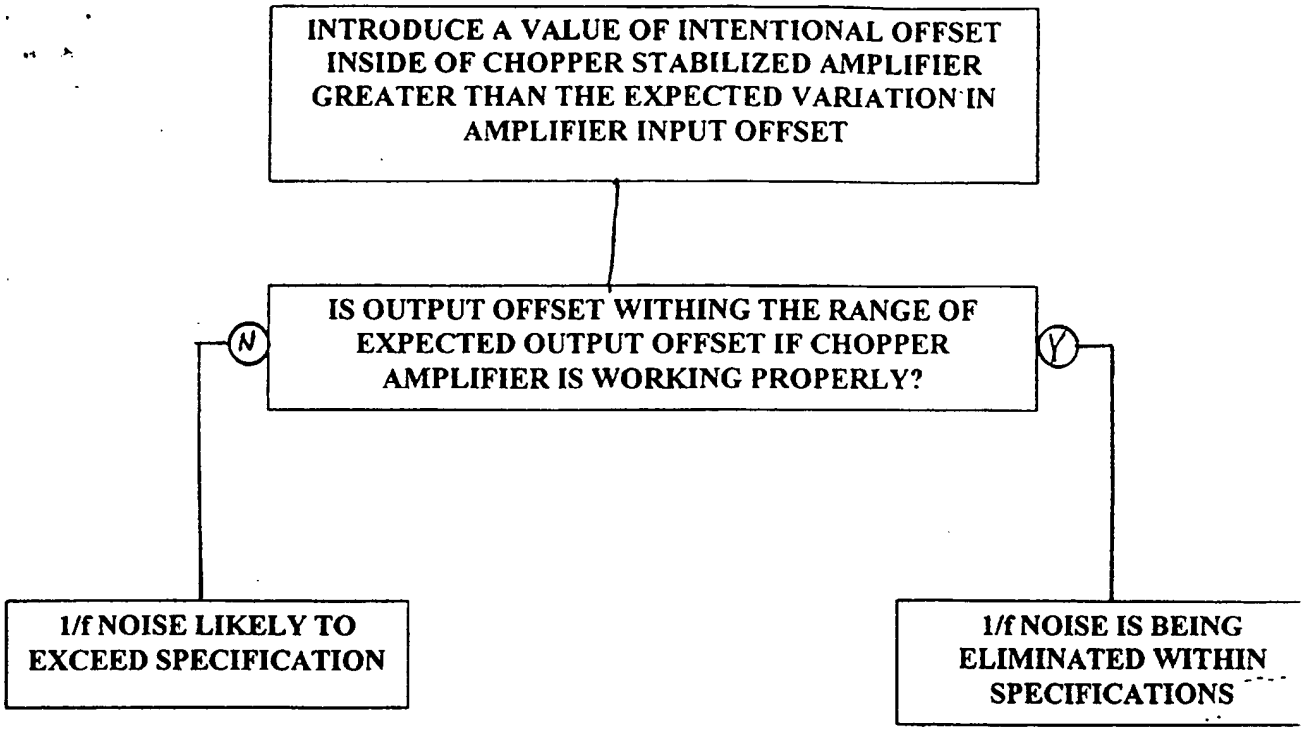

FIGURE 5.1

DOCUMENT - SUBJECT TO COPYRIGHT

Thermocouple Application

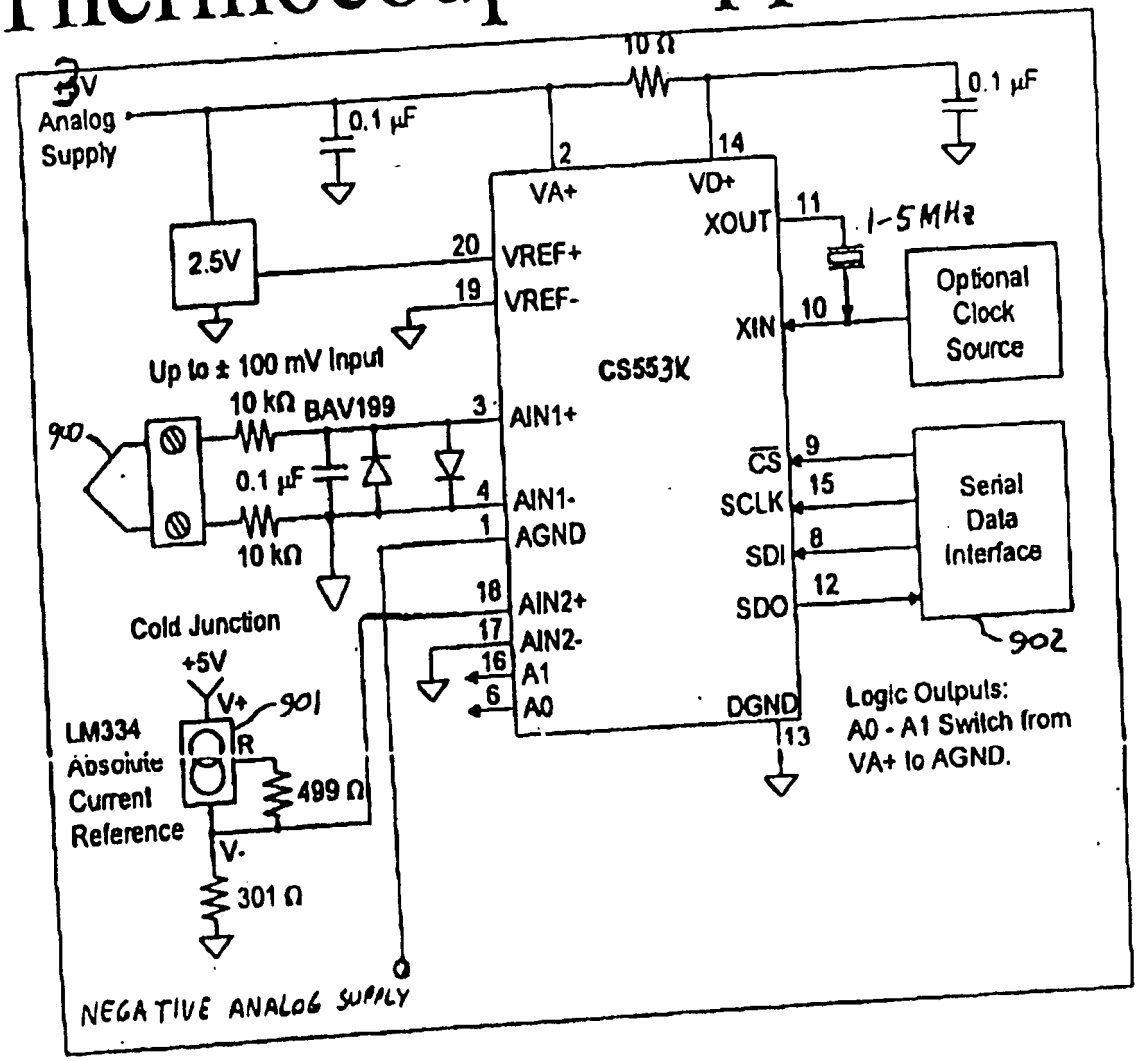

FIGURE 6.1

Bridge Transducer Application

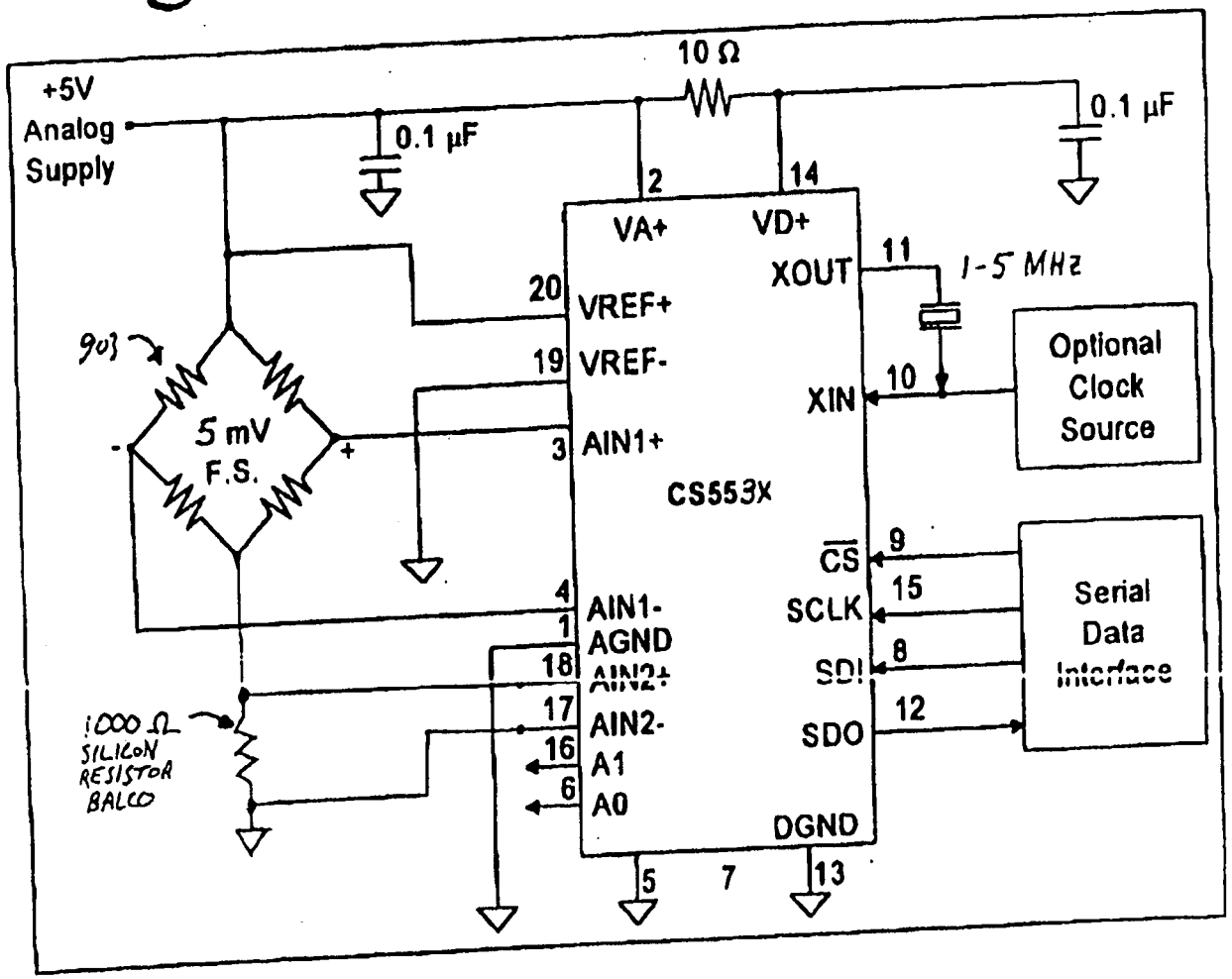

FIGURE 6.2